60 GHz Analog Radio-over-Fiber Single Sideband Transmitter Chipset with 55nm SiGe BiCMOS Driver RFIC and Silicon Photonics Modulator PIC

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Abstract—An all-silicon analog radio-over-fiber transmitter chipset is presented for narrowband operation in the unlicensed 60 GHz V-band for use in low-cost and low-power distributed antenna systems. The chipset consists of a low-noise high-speed quadrature driver RFIC and an EAM based single-sideband I/Q modulator PIC. Resonant matching is used to drive the EAMs which provides 6 dB more gain compared to an on-chip 50 Ω resistive termination. A further 6 dB improvement is had by placing the quadrature hybrid on the RFIC before the output stages compared to implementations that place the hybrid on the PIC. The RFIC consists of a low-noise input stage, gain stages, a hybrid coupler and two output stages while the PIC consists of parallel electro-absorption modulators and thermo-optic phase shifters. A sideband suppression ratio of 25 dB is demonstrated with a full chipset size of 1.1 mm^2 and a power consumption of 45 mW. Succesful optical back-to-back experiments were conducted using various QAM signals.

Index Terms—BiCMOS integrated circuits, Microwave photonics, Silicon photonics, Microwave amplifiers, Millimeter wave radar, Millimeter wave communication.

I. Introduction

THE RF V-band around 60 GHz is an industrially important piece of spectrum as it is the only unlicensed millimeter-wave (mmWave) band below 100 GHz with large bandwidths for communications and sensing applications [1], [2]. Standardization is well underway with both the WiFi alliance and the 3GPP paving the way for high capacity unlicensed standalone networks [3], [4]. Effective use of mmWave frequencies requires the use of small cells as path loss is high, while centralized processing allows for capacity sharing and performance improvement through the use of distributed beamforming [5].

A significant challenge in distributed antenna topologies is the fronthaul links that carry signals to the remote radio heads (RRHs). Fiber-to-the-antenna (FTTA) provides a low-loss fronthaul solution but mmWave RRHs can get quite complex and costly with digital fronthauling standards such as the Common Public Radio Interface (CPRI) [5], [6]. Simpler solutions are needed for low-cost systems that have the potential to be widely deployed. Intermediate frequency-over-fiber

(IFoF) has been promoted as a lower cost solution compared to digital RoF but it requires electrical frequency upconversion at the RRH [7]. IFoF is not suitable for distributed beamforming as the phases of signals from different RRHs are not synchronous after electrical frequency upconversion at the RRH. Optical heterodyning has been shown to be a good solution to relax modulator requirements but complexity is shifted to the optical system [8]. In a two way link, optical heterodyning is only possible for the downlink to the user at the RRH while analog radio-over-fiber (ARoF) is necessary for the uplink [8]. ARoF with optical single sideband modulation (OSSB) has been shown to be a low-cost fronthaul solution for mmWave frequencies while overcoming dispersion based power penalties [9]. OSSB may also be generated by filtering out one of the sidebands using an optical filter but half of the power is lost and the method is not optical wavelength agnostic. A low-cost and highly integrated 60 GHz OSSB ARoF solution is necessary to enable high capacity distributed wireless networks [9].

Silicon based solutions benefit from growth in mass production and offer low cost with steady performance improvements. Leading edge CMOS development has brought significant advances to speciality technologies like SiGe BiCMOS [10] and silicon photonics [11] as a majority of CMOS users move to leading edge nodes and free up tooling capacity for development of speciality nodes. Furthermore, III-V on silicon technologies are expected to improve modulator performance [12] and integrate lasers [13].

Previously published integrated mmWave RoF chips have been demonstrated up to 30 GHz [14] [15] [16]. The 30 GHz OSSB modulator in [14] integrated a quadrature hybrid on the photonic integrated circuit (PIC), which required a driver with a higher single channel output linearity while the hybrid is made with lumped inductors. The lumped inductors scale poorly to higher frequencies due to limited self-resonance. A 28 GHz chipset was demonstrated in [15] which used a GaAs driver while the PIC did not support OSSB. The PIC in [16] supports OSSB but the driver requires external in-phase and quadrature generation off the chipset.

This paper is an extension of our ECOC 2022 paper [17] demonstrating an all-silicon 60 GHz OSSB narrowband photonic transmitter (NBPhoTx) consisting of a SiGe BiCMOS RFIC and a silicon photonics PIC. The PIC consists of parallel electro-absorption modulators (EAMs) and thermo-optic phase shifters which are driven with both in-phase and quadrature components by the RFIC. Sideband suppression of 25 dB

is achieved with a full chipset size of 1.1 mm^2 consuming 45 mW. Succesful optical back-to-back experiments are conducted with QAM signals. Such small and low-power ARoF chipsets can enable mass-produced solutions for large scale distributed antenna arrays.

Section II provides an overview of the chipset while section III briefs EAM modeling and PIC design. Section IV describes RFIC driver design while section V details measurements. Section VI concludes the paper.

II. OVERVIEW

An overview of the proposed OSSB NBPhoTx chipset is shown in Fig. 1, it consists of a low-noise quadrature driver (LNQD) RFIC with a single sideband electro-absorption modulator (1BEAM) PIC. The LNQD RFIC generates I/Q signals from a single input and consists of a low-noise input stage, followed by gain stages, a quadrature hybrid and output stage. The 1BEAM PIC is an I/Q modulator consisting of parallel EAMs followed by thermo-optic phase shifters. The RFIC is manufactured using a 55nm SiGe BiCMOS process while the PIC is manufactured using the iSiPP50G process.
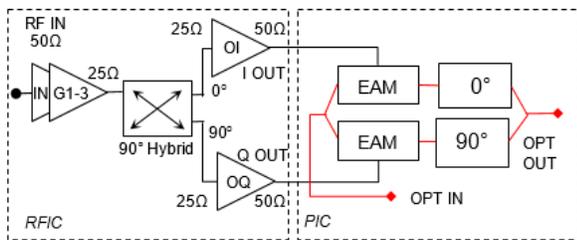
Fig. 1: Overview of the narrowband optical transmitter chipset.

III. EAM MODEL AND PIC DESIGN

EAMs are small and offer high bandwidths compared to Mach-Zehnder modulators (MZMs) that are much longer. Due to their compact nature, EAMs were used in this design. The C-band GeSi EAMs utilize the Franz-Keldysh (FK) effect and have been reported to exhibit a static extinction ratio of 4 dB and a dynamic extinction ratio of 3 dB at 56 GBaud when driven with 2 Vpp [18].

Before designing the driver, a test structure of a single EAM was characterized for small-signal model and static absorption curve. This was done so that the output network of the driver can be resonantly matched to the small signal model of the EAM. The absorption curve was used to decide the bias and driving voltages for good linearity. The small signal model was extracted from 1-port vector network analyzer (VNA) measurements done with a 50 Ω standard VNA up to 67 GHz and is shown in Fig. 2 (a). From the smith chart it can be seen that reflection response is capacitive as it is in the bottom half. A series inductance may be used to resonantly match to this capacitive load for a narrow band of frequencies. Based on this, a driver with an inductive output network was required to conjugate match the capacitive EAM at 60 GHz. The static DC response was modeled using a lab laser at 1550 nm and a DC supply while fiber probes positioned over grating couplers

were used to couple light in and out of the test chip. The results are shown in Fig. 2 (b), based on this it was decided to bias the EAM at -1 V and drive it with a 2 Vpp signal.
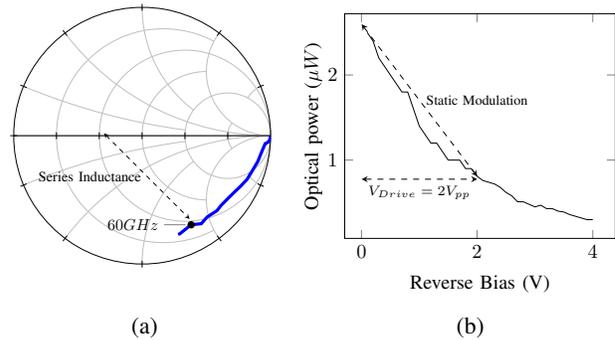
Fig. 2: Characterization of a single EAM test structure (a) S$_{11}$ measured with a 50 Ω VNA (b) Optical power through the test chip at different DC bias voltages at an optical wavelength of 1550 nm.

A schematic of the 1BEAM PIC is shown in Fig. 3 while a layout, micrograph and device under test in Fig. 4. It consists of grating couplers (GC) for input and output as well as 1x2 multi-mode interferometers (MMIs) to split and combine light from two identical arms. Each arm contains an EAM [18] and a doped-silicon thermo-optic phase shifter (PS) [19]. The PIC simulations were done in VPI photonics while the optical PCell based layout design was done using a PIC mask design tool called IPKiss place and route. The final metallization was added using klayout. RF pads were added with ground-signal-ground-signal-ground (GSGSG) configuration with 150 μm pitch for the EAMs while a single pad was used to bias each thermo-optic phase shifter. The return DC current from the phase shifters flowed through the RFIC through the common ground GSGSG pads.
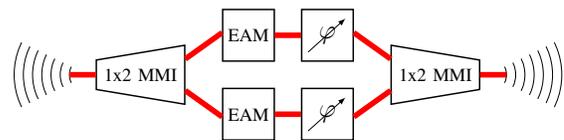
Fig. 3: Schematic of photonic chip.
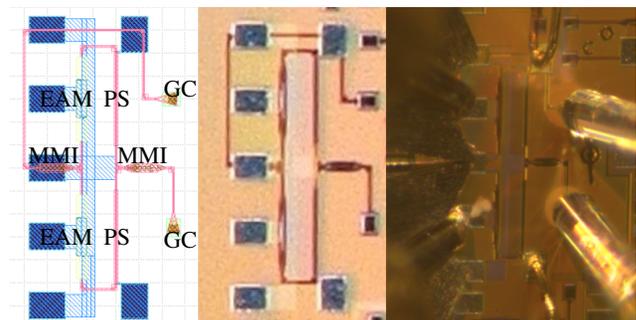
Fig. 4: Layout of photonic chip, manufactured chip and device under test.

IV. DRIVER RFIC DESIGN

In order to drive the 1BEAM PIC effectively, a driver RFIC is proposed that can generate both in-phase and quadrature signals with reasonable swing. The output networks are resonantly matched to the EAMs as shown in Fig. 5 which in this case was provided by wirebond inductance of approximately 250 pH. The EAMs are biased through the RFIC with bias-tee networks capable of sinking large photocurrents from the EAMs in the range of 1 to 3 mA. The quadrature signals are generated before the output stages using a quadrature hybrid.
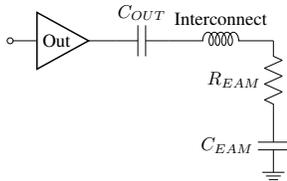
Fig. 5: Simplified schematic of output network.

An overview of low-noise quadrature driver (LNQD) is shown in Fig. 6. The LNQD consists on an input stage (IN), three gain stages (G1-3), a quadrature hybrid and two output stages (OI,OQ). The input impedance of the input stage was 50 Ω and so was the output impedance of the output stage, other than that all the interstage impedances were designed for 25 Ω. This was primarily due to a significant reduction in layout size of the quadrature hybrid designed for 25 Ω as opposed to one designed for 50 Ω using the reduced size method.
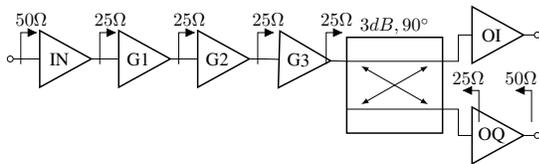
Fig. 6: Overview of low-noise quadrature driver stages.

A. Reduced-size quadrature hybrid

A 60 GHz branch-line quadrature hybrid made with quarter-wavelength transmission-lines (TLs) is large on-chip at as each arm is about 600 μm long. In addition to area related cost penalties, a longer TL also results in more copper losses which increase insertion loss of the component. While meandered TLs [20] can reduce layout area, copper losses are not reduced while adding discontinuities at bends.

A reduced-size branch line hybrid has been proposed by [20] which was found to be suitable and implemented in the LNQD. The method relies on using shorter high-impedance TLs loaded with capacitors as equivalent to quarter-wave TLs. The size reduction is proportional to the characteristic impedance required (Z_0) over the impedance of the TLs used (Z_{TL}). Therefore designing for a Z_0 of 50 Ω with a Z_{TL} of 70 Ω has some area gains but this ratio was maximized in the LNQD with designing for a Z_0 of 25 Ω using a Z_{TL} of 100 Ω. These values were considered optimal due to process design rules restricting how close or how far the ground

plane can be from signal lines which are largely dominated by maintaining reasonable local density for the copper dual-damascene process. An analysis of the sizes is shown in Tab. I.

TABLE I: Size comparison of hybrid implementations.

Implementation	Horizontal	Vertical	Area
Quarter-wave TLs Z_0 = 50 Ω	625 μm	625 μm	0.390 mm^2
Reduced-size Z_0 = 50 Ω	124 μm	256 μm	0.032 mm^2
Reduced-size Z_0 = 25 Ω	98 μm	146 μm	0.015 mm^2

Based on the analytical calculations, a first electromagnetic (EM) model was made and optimized using parametric layout cells of TLs made using the foundry stackup. To further model a realistic layout, an EM cell was made for each corner with attention paid to the grounds on either side of the CPW TL converging. This corner cell was further optimized with TL PCells for each segment. Once optimized, this was finally verified with a full EM simulation of the whole quadrature hybrid layout and further tuned as a full EM cell. A manufactured micrograph is shown in Fig. 7.

Fig. 7: Micrograph of reduced-size branch-line quadrature hybrid.

B. Active gain stages

The input, gain and output stages consist of AC-coupled tuned narrowband common-emitter (CE) amplifiers with emitter degeneration realized using heterojuction bipolar transistors (HBTs). The inductive elements are made using high impedance CPW TLs while MIM capacitors are used for AC-coupling. The transistor size and bias current of the input stage is optimized for low-noise while the gain stages are optimized for high-gain and the output stages are optimized for linearity.

In a CE stage, the real part of the input impedance depends on the length of the emitter TL while the imaginary part of the input impedance is tuned out with the length of the base TL. The output network is matched using a LC stage formed by the collector TL and the output capacitor which also provides DC decoupling between stages. Designing for a 25 Ω internal impedance had a secondary advantage that the emitter TL and the collector TL can be shorter which improves gain and reduces size. Simulations were done using foundry provided circuit RF PCells for the lumped components such as resistors, capacitors and transistors. TLs were modeled
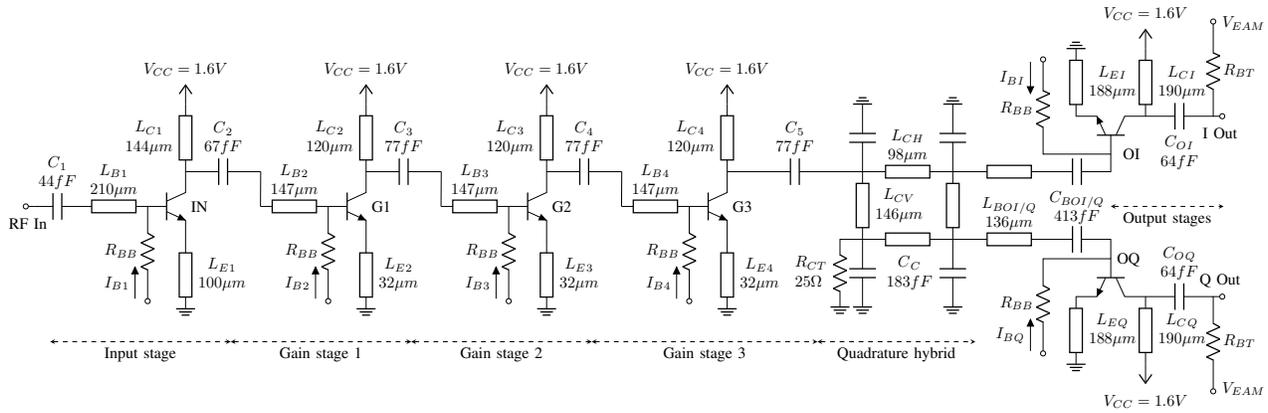
Fig. 8: Simplified schematic of low-noise quadrature driver.

with custom electromagnetic PCells made using the foundry stackup. Simulations indicated a gain of 25 dB and a noise figure of 4 dB. A simplified schematic is shown in Fig. 8 and the manufactured RFIC under test in Fig. 9.

C. Finishing

The chip was finished by adding decoupling, bias-tees, pads, fills and fill-excludes. On-chip 440 fF decoupling capacitors are placed where an AC ground is needed for 60 GHz as well as 20 pF spread over the V_{CC} supply network (omitted from schematic). Bias-tees were placed in the output networks so the EAMs may be biased through the RFIC. A large 300 Ω resistor was used for this, sized to handle the expected EAM photocurrent of 1-3 mA with acceptable voltage drop of up to 1 V at high optical powers. Octagonal pads 50 μm size and 150 μm pitch were used with GSG150 at the input and GSGSG150 at the output. Single pads of the same type were used for DC bias. During finishing, tiling processes that place dummy metal in the passive structures were manually excluded on all metal layers.

V. ASSEMBLY AND MEASUREMENTS

The chips were diced close to the RF pads, thinned to 250 μm and assembled on a PCB with wirebonds. Very short ball-stitch-on-ball (BSOB) shapes were used for the 60 GHz connections while long ball-stitch shapes were used for DC connections. The EAMs were biased through the RFIC while the heaters were biased through the PCB.

A. Driver RFIC characterization

The driver was characterized using VNA measurements calibrated to probe tips as shown in Fig. 9. A plot of the measured gain of both outputs compared to simulations can be seen in Fig. 10. It can be seen that the measured response has shifted which may have been caused by some inaccuracies in modeling of the gain stages. A plot of the phase difference between the two outputs is shown in Fig. 11, this has also shifted by about 5 degrees and can be caused by inaccuracies in modeling the quadrature hybrid. Despite shifting of the gain and phase response, the chip still performs well for this

application. The reflection response of the three ports is shown in Fig. 12 and shows good matching on each port. A power sweep was conducted to measure gain compression and is shown in Fig. 13.
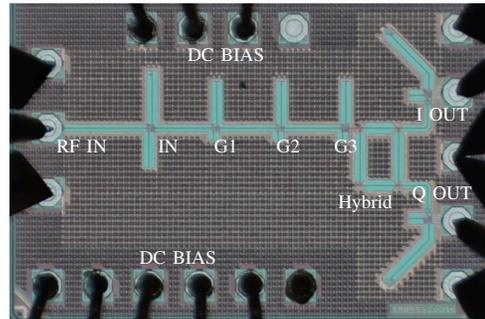
Fig. 9: Low-noise quadrature driver under test.
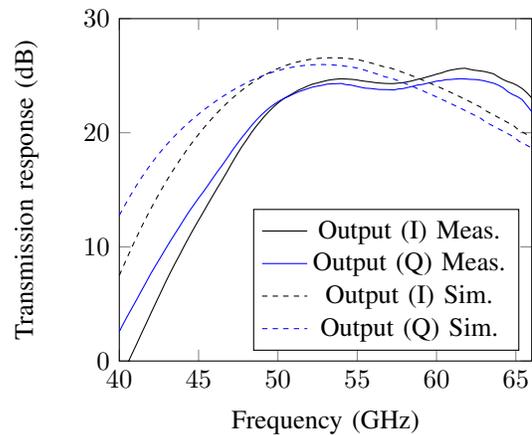
Fig. 10: Measured and simulated frequency responses of quadrature driver outputs.

B. Electro-optic frequency response characterization

The frequency response of the transmitter chipset was characterized as shown in Fig. 14 using a VNA and a high-speed 50 GHz photodiode (Finisar XPD2120RA). The obtained
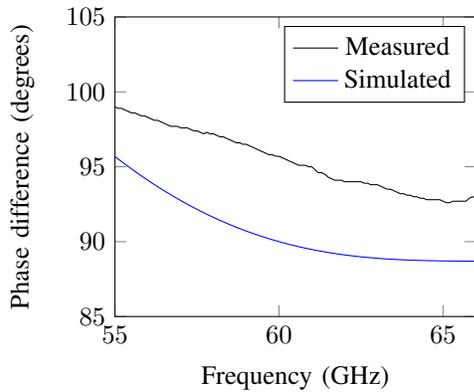
Fig. 11: Phase difference between I and Q outputs of quadrature driver.
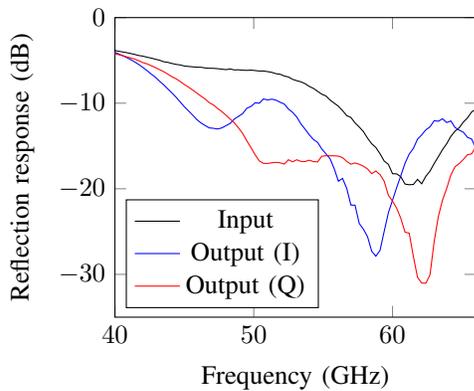
Fig. 12: Measured reflection responses of quadrature driver.
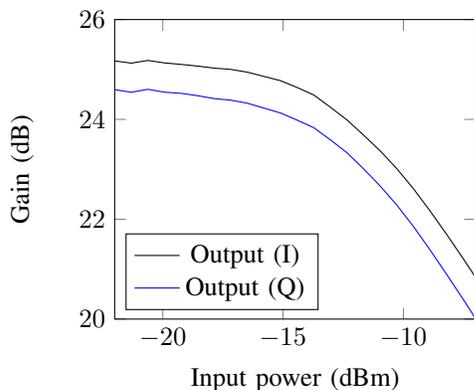
Fig. 13: Measured gain compression of quadrature driver.

response is shown in Fig. 15. The VNA was calibrated to the ends of its RF cables hence this includes the frequency response of the probes as well as the photodiode. This was as expected although the gain is higher at 50 GHz compared to 60 GHz which may have been caused by the frequency response of the probes and the photodiode added together resulting in higher loss at 60 GHz.
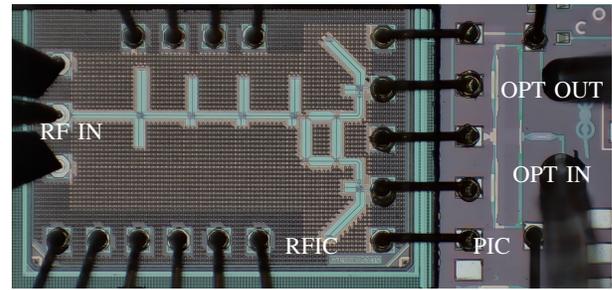
Fig. 14: Narrowband photonic transmitter chipset under test.
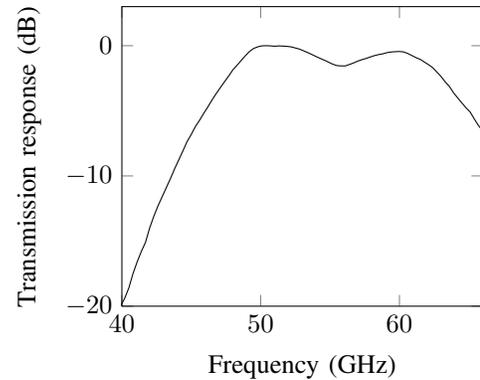
Fig. 15: Measured electro-optical frequency response of narrowband photonic transmitter chipset.

C. Single tone modulation characterization

The single-tone response of the NBPhoTx chipset was characterized using part of the setup shown in Fig. 16 where a 60 GHz input signal was generated using an oscillator (Anritsu MG3696B) and interfaced to the DUT using a GSG probe (Picoprobe 67A). A 1550 nm continuous wave laser source (Tunics T100S-HP) was coupled in and out of the chipset using optical probes positioned over grating couplers. A polarization controller was used to optimize the input optical polarization for maximum optical coupling as the grating couplers are polarization sensitive. The EAMs were biased with -1 V while one of the thermo-optic phase shifters was biased for $90°$ phase shift with 6.9 V which resulted in 10 mW of power through the 4.7 KΩ resistive heater device. The output was observed using an optical spectrum analyser (OSA, Anritsu MS9740A) and the obtained spectrum is shown in Fig. 17. It can be seen that this implementation has a sideband suppression ratio of 25 dB. This result was compared to VPIphotonics transmission maker model of the PIC and a response was fitted. The measured RFIC output phase difference value of $95°$ at 60 GHz was used in the simulation which agreed with the measurement. The second peak is from the nonlinear response of the EAM which was also defined. The carrier to sideband ratio was used to extract the dynamic extinction ratio of each EAM at 60 GHz while driven with 2 Vpp and was found to be 2.8 dB.

D. Optical back-to-back experiments with modulated signals

In order to demonstrate the NBPhoTx with complex modulated ARoF signals, an optical back-to-back experiment was
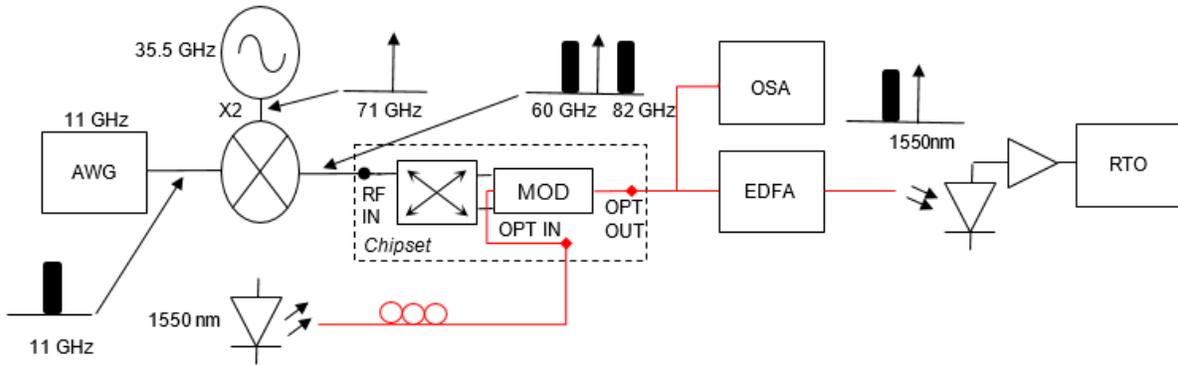
Fig. 16: Setup for optical back-to-back experiments.
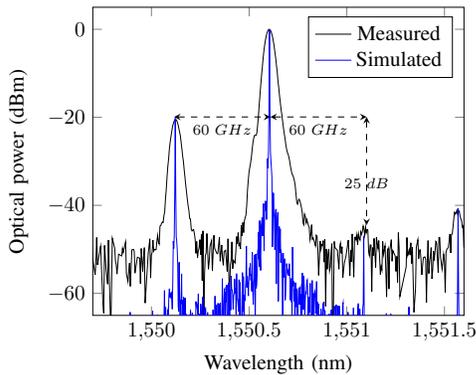
Fig. 17: Optical spectrum of single-tone modulation.

Fig. 18: Obtained constellations from optical back-to-back experiments (a) 100 MBd QAM16 with 8% EVM (b) 200 MBd QAM16 with 10% EVM (c) 500 MBd QPSK with 14% EVM (d) 1 GBd QPSK with 16% EVM.

conducted as shown in Fig. 16. The RF signals were generated at an IF of 11 GHz using an arbitrary waveform generator (AWG, Keysight M8195A) and upconverted to 60 GHz using a waveguide mixer (VDI WR12eCCU) and an oscillator. The output of the mixer was coupled to the chip using GSG probes. The modulated optical signal from the chip was amplified using an erbium doped fiber amplifier (EDFA, Keopsys CEFA-C-HG) and received with a high-speed 50 GHz photodiode (Finisar XPDV2120RA), an amplifier with 10 dB gain (SHF M827A) and a real time oscilloscope (RTO, Lecroy LabMaster 10-65ZiA) where the 60 GHz signal was demodulated in real time. The DSP receive chain on the RTO was made with four blocks, a down converting mixer, IF filter, equalizer and phase estimator. The obtained constellations are shown in Fig. 18.

The link was tested at 100 MBaud and 200 MBaud with QAM16 while QPSK was used at 500 MBaud and 1 GBaud. Due to the signal being very weak and close to the noise floor of the instrument, the generated constellations were very noisy. In addition to the noise, some amplitude drift can also be seen which is caused by the optical fiber shifting over grating couplers. Despite the impairments, successful data demodulation was demonstrated.

A comparison with other published chips is shown in Tab. II. It can be seen that this chipset has the smallest size as well as the lowest power consumption while offering good performance. The current limitations of the chipset are mainly the high loss of grating couplers and the low dynamic extinc-

tion ratio of the EAMs. Performance improvements can be obtained by using lower-loss optical coupling and modulators with higher extinction ratio. The modulated signal experiment was also limited by the assembly as well as signal generation. The mixer used has high conversion loss which is made worse by the long RF coaxial cable needed to reach the chipset. This can be improved by including a mixer closer to the transmitter either on the chip level or the PCB level. Optical fiber probing also causes excess loss and instability and can be improved by better opto-electronic assembly such as fiber gluing. Other than improving opto-electronic assembly, future work includes demonstrating a bi-directional setup, integration with antennas and setting up distributed beamforming experiments.

VI. CONCLUSION

In this paper we propose and experimentally demonstrate an all-silicon 60 GHz mmWave analog radio-over-fiber trans-

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TABLE II: Comparison with radio-over-fiber transmitter chips.

	Frequency	Technology	Size	PIC		Driver			
				Features	Sideband Rejection	Power	OP1dB	OVpp	Gain
This Work	60 GHz	All silicon (wirebond)	1.1 mm^2	OSSB, EAM	25 dB	35 mW	10 dBm	2 V	25 dB
[14]	30 GHz	Silicon PIC (monolithic)	1.7 mm^2	OSSB, Ring mod.	15 dB				
[15]	28 GHz	GaAs + silicon (wirebond)	5.5 mm^2	REAM		124 mW	5.2 dBm		25 dB
[16]	28 GHz	All silicon (wirebond)	2.1 mm^2	OSSB, EAM, SDM		140 mW		2 V	20 dB
[21]	24 GHz	Silicon PIC only	15 mm^2	OSSB, MZM	13 dB				

mitter chipset with optical single sideband modulation. The transmitter chipset consists of a single ended to quadrature driver RFIC and an I/Q modulator PIC. The driver has 25 dB gain and two 2 Vpp outputs for both in-phase and quadrature signals. The modulator PIC has two parallel EAMs with thermo-optic phase shifters. They are assembled on a PCB with very short wirebonds for the 60 GHz connections. The transmitter chipset has a sideband suppression of 25 dB and was demonstrated with complex modulated RF signals.

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